REMARKS/ARGUMENTS

This amendment is submitted in response to the Final Rejection dated October 13, 2004. After entry of this amendment, claims 11-15 will remain pending in the application. Claim 11 has been amended in order to further clarify the instant invention in view of the prior art. Amended claim 11 clearly defines the present invention, describes the characteristics, and further distinguishes features of the present invention from the cited references. The amendment is supported by the specification, on page 3, lines 24-26, page 7, lines 8-10, and by Figures 1(m) and 2. No new matter has been added.

Reconsideration and allowance is respectfully requested in view of the amendments made and the remarks made below.

1. Rejections under 35 U.S.C. §103(a)

The Examiner rejected Claims 11-15 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,614,747 to Ahn et al (hereinafter "Ahn"). The Applicant respectfully submits that Ahn does not teach or suggest each and every limitation of claims 11-15, and therefore a case of *prima facie* obviousness has not been established. Additionally the Applicant submits that the instant invention results in a device that fulfills a long felt need in the art that further renders the instant invention non-obvious in view of Ahn.

To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). "All words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 265 USPQ 494, 496 (CCPA 1970). If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. *In re Fine,* 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

Newly amended claim 11, requires an Electrically Erasable Programmable Read-Only Memory (EEPROM) having a silicone substrate 100 having a source/drain region (114, 113), a tunnel oxide layer 107 disposed over the silicone substrate 100, a select gate 104 disposed over the tunnel oxide layer 107, wherein the select gate 104 is defined by a conductive layer 102 covered with a first insulated material 103 thereon and comprises a sidewall made of a second

insulated material 106, a single floating gate 111 aligned to one side of the select gate 104, a third insulated material 112 contacted with the tunnel oxide layer 107 and the floating gate 111 and disposed over the select gate 104, and a control gate 116 formed on the third insulated material 112 in a way that the third insulated material 112 mounted above the source region 114 is exposed. This structure can be seen in Fig. 1(m). Furthermore, claim 15 requires having the control gate formed on the third insulated material, wherein the control gate "partially covers said third insulated material." The Applicant respectfully submits that Ahn does not disclose having a select gate disposed over the tunnel oxide layer.

Ahn discloses a flash EEPROM cell having a select gate oxide layer, a select gate, and a dielectric oxide layer formed in stacks on a selected region of a p-type substrate. Ahn also discloses having a tunnel oxide layer, a floating gate, a drain region, a source region, an inter-poly oxide layer and a control gate. The tunnel oxide layer 12 is formed on one sidewall of the select gate oxide layer 18, the select gate 20 and the dielectric oxide layer 22 and on a selected region of the p-type substrate extended below from the sidewall. The floating gate 13 is formed on the tunnel oxide layer. Tunnel oxide layer 12 is disposed over substrate 11 and forms a sidewall of select gate 20. Select gate 20 is disposed over select gate oxide layer 18. Select gate 20 is not disposed over tunnel oxide layer 12. The drain region and a source region are formed on the p-type substrate, the inter-poly oxide is formed on the entire structure after the formation of said floating gate, and the control gate is formed on the inter-poly oxide layer in a way that a portion of the inter-poly oxide 14 on the drain region 16 and the source region 17 is exposed. This is shown in Figs. 3E and 4.

In the Office Action, referring to Fig. 3E of Ahn, it is stated that "tunnel oxide layer 12 [is] disposed over said substrate; [and] a select gate 20 [is] disposed over said tunnel oxide layer." However, this is not shown in FIG. 3E of Ahn. Instead, select gate 20 is disposed over select gate oxide layer 18, not over tunnel oxide layer 12. Tunnel oxide layer 12 forms a sidewall of select gate 20. Claims 11 and 15 require having, "a tunnel oxide layer disposed over said silicon substrate; a select gate disposed over said tunnel oxide layer, wherein said select gate is defined by a conductive layer covered with a first insulated material thereon and comprises a sidewall made of a second insulated material." Ahn clearly does not meet this limitation.

Furthermore, the Office Action states that the, "sidewall [is] made of a second insulated material 12." In the Applicant's disclosure and claims the second insulated material is a separate element from the tunnel oxide layer. Additionally, in the Applicant's invention, tunnel dioxide layer 107 runs the entire length of the substrate layer and does not form a sidewall as the tunnel dioxide layer in Ahn does. The Office Action's characterization of the tunnel dioxide layer as also being the second insulated material fails to meet the limitations of the claims since the claims require two separate structures which cannot be met by reference to a single structure in Ahn as being both structures as required by the claims.

Therefore the Applicant respectfully submits that a *prima facie* case for obviousness has not been established since not all of the limitations of claim 11 are taught or suggested by Ahn. The Applicant submits that independent claims 11 and 15 are in condition for allowance, and claims 12-14 are allowable by virtue of their dependence on independent claim 11.

The Applicant further submits that the instant invention satisfies a long felt need in the art by providing an EEPROM structure that is capable of being reduced in size while still maintaining its useful characteristics.

Figure 3E, in Ahn, shows a similar type of structure to that of the present invention, including a floating gate on one side of the select gate. However, Ahn's device can be clearly differentiated from the features and the functions of the present invention.

Primarily the structure of the control gate in Ahn and the present application are different. In Ahn's flash EEPROM cell, the inter-poly oxide layer is formed on the entire structure after the formation of the floating gate, and the control gate is formed on the inter-poly oxide layer in such a way that a portion of the inter-poly oxide layer 14 on the drain region 16 and the source region 17 is exposed. The size of such a control gate leads to a larger flash EEPROM cell. If the flash EEPROM cell is too large, its usefulness decreases since its ability to operate within miniaturized components and electronic circuits decreases.

In the past, a split gate cell was useful in that it avoided the over-erase problem, however the split gate cell is not widely used due to the complexity of manufacturing such split gate cells, and the relatively large size of the resultant product. Therefore it is important to reduce the size of the split gate cell as much as possible for more widespread application. Although the structure of the EEPROM provided in the present invention and Ahn's flash EEPROM cell both

focus on providing an EEPROM with a small size without the over-erase problem, the structure of the EEPROM provided in the Applicant's invention is better than that of Ahn's flash EEPROM cell by being able to provide an EEPROM that has a much smaller size than than of Ahn.

Although one may think that there is only a minor difference between these two control gates, the design of the control gate for a flash EEPROM cell in the Applicant's invention leads to a powerful effect in respect to scaling down the size without losing the program disturb immunity of a flash EEPROM cell. Supplemental drawings, Figs. 1 and 2, provided below for explanatory purposes, demonstrate the differences between Ahn's device and the Applicant's invention. Figs. 1 are 2 are lateral views of the structure of an EEPROM according to the Applicant's invention (Fig. 1) and of an EEPROM cell according to Ahn (Fig. 2). The exposed region above the drain region, which is defined by the symbol x in Fig. 1 is the same as that in Fig. 2. However, Ahn's control gate is formed on the inter-poly oxide layer in a way that a portion of the inter-poly oxide layer 14 on the drain region 16 is exposed, therefore the control gate will occupy a volume, which is defined be the symbol y. This results in Ahn's EEPROM cell having a larger size. The structural differences of the control gates between the Applicant's invention and Ahn's device result in a dramatic difference with respect to the overall size of the device.

The overall reduction in device size made possible by the Applicant's invention provides increased benefits. Some of the advantages include having the space occupied capable of being reduced for other components, which can result in optimizing the manufacturing of the memory device.

To sum up the above comparisons, the elements of the structure of the EEPROM of the Applicant's invention are not only different from those of the Ahn flash EEPROM cell, but also result in a device that has greater benefits than those of Ahn's flash EEPROM cell. It should also be noted that having a device that can be constructed from simple processing steps, without the over-erasing problem and further resulting in a small size in the EEPROM structure is a very desirable product in the field. Although the device disclosed in Ahn is directed toward the goal of eliminating the over-erasing problem and scaling down the size at the same time, it does not accomplish the goal to the same degree that the Applicant's invention has. The Applicant's invention provides an EEPROM structure with a cell size smaller than a traditional split gate structure without sacrificing program disturb immunity. Ahn does not accomplish a similar result.

In view of the above, the Applicant's invention clearly provides a useful structure to fulfill long-felt needs in the field. Therefore, the Applicant submits that claims 11-15 are non-obvious in view of Ahn for these additional reasons.

2. Conclusion

The Applicant has made an earnest effort to place this application in condition for allowance. If the Examiner feels that a telephone interview would expedite prosecution of this patent application, he is respectfully invited to telephone the undersigned at 215-599-0600.

Respectfully submitted,

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